UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/045,288	10/18/2001	Nils Ramon Marchant	010327-003700US	4470

20350 7590 03/11/2004

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	7

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/045,288	MARCHANT ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-30 are presented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 10/18/2001 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Erimli et al., U.S. Patent 6,618,390 B1, in view of McKenney., U.S. 2002/0194436 A1.

Regarding claims 1,11 and 21, Erimli teaches that a method of caching free cell pointers pointing to memory buffers configured to store data traffic of network connections, the method comprising:

storing free cell pointers into a pointer random access memory (RAM) (it is taught as storing free cell pointers into the free buffer queue 64; col.6, lines 11-12; col.7, lines 49-51; col.8, lines 15-18), wherein each free cell pointer points to a memory buffer that is vacant and available for storing data traffic (col.7, lines 53-56 and col.8, lines 15-17);

temporarily storing at least one free cell pointer into internal cache configured to assist in lowering a frequency of reads from and writes to the pointer RAM;

receiving a request (col.8, lines 59-61) from an external integrated circuit (it is taught as the switching subsystem 42) for free cell pointers;

sending free cell pointers to queues (it is taught as a queuing logic 74) of the external integrated circuit, wherein each free cell pointer in a queue (col.7, lies 49-53) is configured to become a write cell pointer (col.8, lines 4-11);

receiving at least one write cell pointer (col.8, lines 4-6) and a corresponding cell descriptor (col.8, lines 33-35, it is taught as the forwarding descriptor) from the external integrated circuit (col.8, lines 20-42); and

calculating free cell pointer counter values in order to keep track of the free cell pointers(col.9, lines 13-29).

Erimli does not teach that temporarily storing at least one free cell pointer into internal cache configured to assist in lowering a frequency of reads from and writes to the pointer RAM;

However, McKenney teaches that temporarily storing at least one free cell pointer into internal cache (it is taught as the pointers store in the odd or eve numbered cache line, col.3, section 0030, last 8 lines) configured to assist in lowering a frequency of reads from and writes to the pointer RAM (this is the purpose of using cache to speed up the access operation);

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of McKenney in the system of Erimli and have the cache storing free cell pointer because cache memory has the advantages of speeding up the memory access operation, therefore, latency is significantly decreased, these are the purpose of using cache, McKenney resolved Erimli's problem which are the latency and bandwidth problems (col.2, lines 37-39).

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claims 2,12 and 22, Erimli teaches that the pointer random access memory (RAM) (free buffer queue 64) is external to controller circuitry (Fig.3, scheduler 80) configured to control the steps of the method (col.7, lines 57-61).

Regarding claims 3,13 and 23, Erimli teaches that the external integrated circuit is an egress backplane interface subsystem (EBISS) (the switching subsystem 42), and

the queues of the external integrated circuit are first in, first out (FIFO) queues (col.6, lines 1-5).

Regarding claims 4,14 and 24, Erimli teaches further comprising sending read cell pointers with corresponding cell descriptors to the external integrated circuit (col.6, lines 43-45), wherein each read cell pointer points to a memory buffer that has been read (col.6, lines 52-62) and that is free to be reused (col.7, lines 9-11).

Regarding claims 5,15 and 25, Erimli teaches that the step of storing free cell pointers comprises:

storing odd free cell pointers in an odd free list of the pointer RAM (col.10, lines 4-5, it is taught as the first frame buffer 410A); and storing even free cell pointers in an even free list of the pointer RAM (coll10, lines 5-6, it is taught as a subsequent frame buffer 410B).

Regarding claims 6,16 and 26, McKenney teaches that the step of temporarily storing free cell pointers comprises:

storing odd free cell pointers in an odd free space of internal cache (col.3, section 0030, last 6 lines); and

storing even free cell pointers in an even free space of internal cache (col.3, section 0030, last 6 lines).

Regarding claims 7, 17 and 27, Erimli teaches that the step of calculating free counter values comprises performing at least one of:

incrementing a free counter value to account for a cell pointer that has been sent to the pointer RAM (col.9, lines 17-21); and

decrementing a free counter value to account for a cell pointer that has been received from the pointer RAM (col.7, lines 43-46).

Regarding claims 8,18 and 28, Erimli teaches that the step of calculating free counter values comprises determining that a free counter value of internal cache is above a high threshold, and wherein the method further comprises writing a block of cell pointers in a burst to the pointer RAM (col.15, lines 27-32 and lines 42-49).

Regarding claims 9,19 and 29, Erimli teaches that the step of calculating free counter values comprises determining that a free counter value of internal cache is below a low threshold, and wherein the method further comprises reading a block of free cell pointers in a burst from the pointer RAM (col.15, lines 32-35 and lines 49-55).

Regarding claims 10,20 and 30, Erimli teaches that the step of calculating free counter values comprises determining that a free counter value of internal cache is above an overload threshold, and wherein the method further comprises temporarily blocking storing of additional free cell pointers into internal cache (col.15, lines 35-38 and lines 64-67).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Klausmeier et al.,	US 6487202 B1
Armangau et al.	US 6549992 B1

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Mano Padmanabhan 3/5/04

Jasmine Song

Patent Examiner

March 2, 2004

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100